

A new pinched-off cold-FET method to determine parasitic capacitances of FET equivalent circuits

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A new pinched-off cold FET method to extract the parasitic capacitances of FETs is proposed in this paper. The method is based on a physically meaningful depletion-layer model and the theoretical analysis of the two-port network for the pinched-off cold FETs. The parasitic gate capacitance (C_{pg}) and the parasitic drain capacitance (C_{pd}) of FETs are extracted using the linear regression technique associated with the frequency responses of Y-parameters. The extraction method can be applied to the small-signal equivalent-circuit modeling of the FETs including MESFETs, heterojunction FETs, and high-electron-mobility transistors. According to the new analytical method, the simulated S-parameters exhibit great agreement with the measured S-parameters for the equivalent-circuit models of FETs.

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